CLAIMS

1. An apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said apparatus comprising:

an input interface over which the multiplexed signal can be received;

at least one polarization demultiplexer for receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer.

2. The apparatus of claim 1, wherein the multiplexed signal is characterized by a bit rate, the recovered clock signal having a frequency of one-half the bit rate.

3. The apparatus of claim 2, wherein the control signal is generated so as to maximize amplitude of the recovered clock signal.

4. The apparatus of claim 1, wherein the control signal is generated so as to maximize amplitude of the recovered clock signal.

5. The apparatus of claim 1, wherein the control signal is a feedback signal.

6. The apparatus of claim 1, wherein the multiplexed signal is a cross-polarization multiplexed signal.

7. The apparatus of claim 1, wherein a first component signal of the multiplexed signal is characterized by a first polarization and a second component signal of the multiplexed signal is characterized by a second polarization different than the first polarization.

8. The apparatus of claim 1, wherein the multiplexed signal is a time-division multiplexed (TDM) combination of the component signals.

9. The apparatus of claim 8, wherein adjacent component signals within the TDM signal have different polarizations.

10. The apparatus of claim 8, wherein adjacent component signals within the TDM signal have orthogonal polarizations.

11. The apparatus of claim 1, wherein the polarization demultiplexer comprises a polarization beam splitter.

12. The apparatus of claim 1, wherein the polarization demultiplexer comprises a polarization transformer.

13. The apparatus of claim 12, wherein the polarization transformer comprises a plurality of cascaded retardation waveplates.

14. The apparatus of claim 1, wherein the polarization demultiplexer generates a pair of polarization demultiplexed signals.

15. The apparatus of claim 1, further comprises a time demultiplexer for receiving the polarization demultiplexed signal and generating therefrom at least one time and polarization demultiplexed signal.

16. The apparatus of claim 15, wherein the at least one time and polarization demultiplexed signal is a recovered version of one of the component signals.

17. The apparatus of claim 15, wherein the time demultiplexer comprises at least one electro-optical (EO) modulator for generating the at least one time and polarization demultiplexed signal.

18. The apparatus of claim 17 wherein the polarization demultiplexed signal is aligned to the input of the EO modulator.

19. The apparatus of claim 17, wherein the EO modulator is a 1x2 modulator having one input and two outputs.

20. The apparatus of claim 17, wherein the EO modulator comprises an RF input, a phase-adjusted version of the recovered clock signal being applied to the RF input.

21. The apparatus of claim 20, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating

an error signal used to adjust the phase of the phase-adjusted version of the recovered clock signal.

22. The apparatus of claim 20, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the clock signal.

23. The apparatus of claim 17, wherein the EO modulator comprises an RF input, a phase-adjusted version of a sub-harmonic of the recovered clock signal being applied to the RF input.

24. The apparatus of claim 23, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating an error signal used to adjust the phase of the phase-adjusted version of the sub-harmonic of the recovered clock signal.

25. The apparatus of claim 23, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the sub-harmonic of the clock signal.

26. The apparatus of claim 17, wherein the EO modulator comprises an RF input, a phase-adjusted version of a harmonic of the recovered clock signal being applied to the RF input.

27. The apparatus of claim 26, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating

an error signal used to adjust the phase of the phase-adjusted version of the harmonic of the recovered clock signal.

28. The apparatus of claim 26, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the harmonic of the clock signal.

29. The apparatus of claim 17, wherein the EO modulator comprises a bias input, a bias signal applied to the bias input perturbing the bias of the EO modulator from quadrature.

30. An apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said apparatus comprising:

an input interface over which the multiplexed signal can be received;

a polarization demultiplexing stage for receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

a time demultiplexing stage for receiving the at least one polarization demultiplexed signal and time demultiplexing the polarization demultiplexed signal to generate at least one time and polarization demultiplexed signal.

31. The apparatus of claim 30, further comprising a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer.

32. The apparatus of claim 31, wherein the control signal is generated so as to maximize amplitude of the recovered clock signal.

33. The apparatus of claim 30, wherein the control signal is generated so as to maximize amplitude of the recovered clock signal.

34. The apparatus of claim 30, wherein the control signal is a feedback signal.

35. The apparatus of claim 30, wherein the multiplexed signal is characterized by a bit rate, the recovered clock signal having a frequency of one-half the bit rate.

36. The apparatus of claim 29, wherein the multiplexed signal is a cross-polarization multiplexed signal.

37. The apparatus of claim 36, wherein a first component signal of the multiplexed signal is characterized by a first polarization and a second component signal of the multiplexed signal is characterized by a second polarization different than the first polarization.

38. The apparatus of claim 30, wherein the multiplexed signal is a time-division multiplexed (TDM) combination of the component signals.

39. The apparatus of claim 30, wherein the polarization demultiplexing stage comprises a polarization beam splitter.

40. The apparatus of claim 30, wherein the polarization demultiplexing stage comprises a polarization transformer.

41. The apparatus of claim 40, wherein the polarization transformer comprises a plurality of cascaded retardation waveplates.

42. The apparatus of claim 30, wherein the polarization demultiplexing stage generates a pair of polarization demultiplexed signals.

43. The apparatus of claim 30, wherein the at least one time and polarization demultiplexed signal is a recovered version of one of the component signals.

44. The apparatus of claim 38, wherein adjacent component signals within the TDM signal have different polarizations.

45. The apparatus of claim 38, wherein adjacent component signals within the TDM signal have orthogonal polarizations.

46. The apparatus of claim 30, wherein the time demultiplexing stage comprises at least one electro-optical (EO) modulator for generating the at least one time and polarization demultiplexed signal.

47. The apparatus of claim 46, wherein the polarization demultiplexed signal is aligned to the input of the EO modulator.

48. The apparatus of claim 46, wherein the EO modulator is a 1x2 modulator having one input and two outputs.

49. The apparatus of claim 46, wherein the EO modulator comprises an RF input, a phase-adjusted version of the recovered clock signal being applied to the RF input.

50. The apparatus of claim 49, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating an error signal used to adjust the phase of the phase-adjusted version of the recovered clock signal.

51. The apparatus of claim 49, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the clock signal.

52. The apparatus of claim 46, wherein the EO modulator comprises an RF input, a phase-adjusted version of a sub-harmonic of the recovered clock signal being applied to the RF input.

53. The apparatus of claim 52, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating an error signal used to adjust the phase of the phase-adjusted version of the sub-harmonic of the recovered clock signal.

54. The apparatus of claim 52, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the sub-harmonic of the clock signal.

55. The apparatus of claim 46, wherein the EO modulator comprises an RF input, a phase-adjusted version of a harmonic of the recovered clock signal being applied to the RF input.

56. The apparatus of claim 55, further comprising an error signal generating device for receiving the at least one time and polarization demultiplexed signal and generating an error signal used to adjust the phase of the phase-adjusted version of the harmonic of the recovered clock signal.

57. The apparatus of claim 53, wherein the phase of the recovered clock signal is dithered to produce the phase-adjusted version of the harmonic of the clock signal.

58. An apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization and including a data signal pattern, said apparatus comprising:

an input interface over which the multiplexed signal can be received;

at least one polarization demultiplexer for receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

at least one receiver associated with one of a plurality of data signal patterns, the receiver analyzing the data signal pattern of a component signal recovered from the multiplexed signal to determine if the data signal pattern matches the data signal pattern associated with the at least one receiver, the at least one receiver providing a feedback signal indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one

receiver, the feedback signal being used to adjust the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver.

59. The apparatus of claim 58, wherein the adjustment of the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver includes rotating the polarization of the at least one polarization demultiplexed signal to an orthogonal state.

60. The apparatus of claim 58, further comprising a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a clock signal, the clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer.

61. The apparatus of claim 58, further comprising a time demultiplexer for receiving the polarization demultiplexed signal and generating therefrom at least one time and polarization demultiplexed signal.

62. The apparatus of claim 61, wherein the at least one time and polarization demultiplexed signal is a recovered version of one of the component signals.

63. The apparatus of claim 61, wherein the time demultiplexer comprises at least one electro-optical (EO) modulator for generating the at least one time and polarization demultiplexed signal.

64. The apparatus of claim 63, further comprising a clock recovery circuit for receiving the polarization demultiplexed signal and recovering therefrom a clock signal, the clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer.

65. The apparatus of claim 64, wherein the EO modulator comprises an RF input, a phase-adjusted version of the clock signal being applied to the RF input.

66. The apparatus of claim 65, wherein, if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver, the phase of the clock signal applied to the RF input is adjusted 180 degrees.

67. An apparatus for demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said apparatus comprising:

an input interface over which the multiplexed signal can be received;

a clock recovery circuit for receiving the multiplexed signal and recovering therefrom a clock signal;

an electro-optical modulator for receiving the multiplexed signal and generating at least one demultiplexed signal therefrom, the electro-optical modulator including an RF input and a bias input, the RF input receiving a phase-adjusted version of the clock signal;

a detector circuit for detecting the at least one demultiplexed signal from the electro-optical modulator and generating therefrom an error signal; and

a processor for receiving the error signal from the detector circuit and generating a control signal based on the error signal, the control signal being used

to adjust the phase of the clock signal applied to the RF input of the electro-optical modulator.

68. The apparatus of claim 67, wherein the error signal is a signal having a frequency equal to a data rate of the demultiplexed signal.

69. The apparatus of claim 68, wherein the control signal is generated to adjust the phase of the clock signal to maximize a portion of the error signal at the data rate of the demultiplexed signal.

70. The apparatus of claim 67, wherein the phase of the clock signal applied to the RF input of the electro-optical modulator is periodically varied at a dither rate.

71. The apparatus of claim 70, wherein the control signal is generated to adjust the phase of the clock signal to minimize a portion of the error signal that is at the dither rate.

72. The apparatus of claim 67, wherein the control signal is generated to adjust the phase of the clock signal to optimize an attribute of the demultiplexed signal.

73. The apparatus of claim 72, wherein the attribute is error rate in the demultiplexed signal.

74. The apparatus of claim 72, wherein the optimization is done by decoding information in the demultiplexed signal.

75. The apparatus of claim 74, wherein the decoded information is error correction information.

76. The apparatus of claim 74, wherein the decoded information is forward error correction (FEC) information.

77. A method of demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said method comprising:

receiving the multiplexed signal over an interface;

receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

receiving the polarization demultiplexed signal and recovering therefrom a recovered clock signal, the recovered clock signal being used to generate a control signal, the control signal being used to adjust the polarization demultiplexer.

78. A method of demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said method comprising:

receiving the multiplexed signal over an interface;

receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

receiving the at least one polarization demultiplexed signal and time demultiplexing the polarization demultiplexed signal to generate at least one time and polarization demultiplexed signal.

79. A method of demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization and including a data signal pattern, said method comprising:

receiving the multiplexed signal over an interface;

receiving the multiplexed signal from the input interface and generating therefrom at least one polarization demultiplexed signal of a first polarization; and

providing at least one receiver associated with one of a plurality of data signal patterns, the receiver analyzing the data signal pattern of a component signal recovered from the multiplexed signal to determine if the data signal pattern matches the data signal pattern associated with the at least one receiver, the at least one receiver providing a feedback signal indicative of whether the analyzed data signal pattern matches the data signal pattern associated with the at least one receiver, the feedback signal being used to adjust the polarization demultiplexer if the analyzed data signal pattern does not match the data signal pattern associated with the at least one receiver.

80. A method of demultiplexing a multiplexed signal, said multiplexed signal being a combination of a plurality of component signals, each component signal being characterized by a polarization, said method comprising:

receiving the multiplexed signal over an interface;

receiving the multiplexed signal and recovering therefrom a clock signal;

providing an electro-optical modulator for receiving the multiplexed signal and generating at least one demultiplexed signal therefrom, the electro-optical modulator including an RF input and a bias input, the RF input receiving a phase-adjusted version of the clock signal;

providing a detector circuit for detecting the at least one demultiplexed signal from the electro-optical modulator and generating therefrom an error signal; and

providing a processor for receiving the error signal from the detector circuit and generating a control signal based on the error signal, the control signal being used to adjust the phase of the clock signal applied to the RF input of the electro-optical modulator.